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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,435	01/10/2002	Takashi Kariya	217883US3PCT	6548

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1940 DUKE STREET  
ALEXANDRIA, VA 22314

EXAMINER
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GOFF II, JOHN L

ART UNIT	PAPER NUMBER
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1733

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/030,435

Applicant(s)

KARIYA, TAKASHI

Examiner

John L. Goff

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/12/05 has been entered. The request for refund has been noted and forwarded to the Office of Finance.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### ***Claim Rejections - 35 USC § 103***

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gerber et al. (U.S. Patent 5,401,913) in view of either one of Bohn (U.S. Patent 6,537,412) or Johnston (U.S. Patent 5,153,050) and Enomoto et al. (WO 98/56220 with U.S. Patent 6,518,513 used as a translation).

Gerber et al. disclose a method for manufacturing a multilayer circuit board. Gerber et al. teach forming a single circuit board by providing an insulating layer (e.g. 10 of Figure 1), forming a conductor layer (e.g. copper foil) on one side of the insulating layer (e.g. 12 of Figure 1), forming a via hole (e.g. 18 of Figure 5) (e.g. formed by laser processing) through the insulating layer to the conductor layer, filling at least part of the via hole with a first plated

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conductor material (e.g. 20 of Figure 6) wherein at least part of the upper surface of the conductor material is lower than the upper surface of the insulating substrate, etching the conductor layer to form a conductor circuit (e.g. 12 and 16 of Figures 6 and 7), forming a conductive bump (e.g. 22 of Figure 8) on the first conductor material from a second conductive material having a low melting point such that the bump projects from the upper surface of the insulating substrate, and placing a bonding layer (e.g. 24 of Figure 9) over the conductive bump (Figures 1-8 and Column 3, line 68 and Column 4, lines 1, 9-12, 42-43, 54-58, and 63-68 and Column 5, lines 1-5, 11-13, and 15-21). Gerber et al. teach manufacturing a multilayer circuit board by applying heat and pressure to a multilayer stack comprising a plurality of single circuit board layers (as described above) and a lower outermost copper conductor layer (e.g. 50 of Figure 9 wherein the conductor layer has a uniform thickness throughout) to form a multilayer circuit board wherein the conductive bump of each circuit board is connected to the conductor layer of an adjacent circuit board (Figures 9 and 10 and Column 5, lines 46-55 and 61-68 and Column 6, lines 1-3 and 12-21 and Column 7, lines 18-28). It is noted Figures 9 and 10 of Gerber et al. do not depict an upper outermost copper conductor layer. However, Gerber et al. teach the multilayer circuit board of Figure 9 is connected on its upper side to substrates including a copper conductor layer to form an integral, operable multilayer circuit board (Figure 11 and Column 5, lines 63-68 and Column 6, lines 1-3 and 58-65 and Column 7, lines 18-23). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include on the multilayer circuit board taught by Gerber et al. (See Figure 9) during pressing an upper outermost conductor layer (e.g. copper foil) and layer of interposed adhesive to form an integral, operable (i.e. electrically interconnected) conventional multilayer circuit board

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substrate wherein the upper and lower outermost conductor layers are etched following pressing to form conductor circuits as this was the conventional technique in the art for forming multilayer circuit boards of the type required by Gerber et al. as shown for example by either one of Bohn or Johnston. Further, Gerber et al. are silent as to how the first conductor material is plated. It would have been obvious to one of ordinary skill in the art at the time the invention was made to plate the first conductor as taught by Gerber et al. using a well known electroplating technique of using the conductor layer as an electrode and covering the non-plated side of the conductor layer with a protective layer in order to plate the conductor without altering the thickness of the non-plated side as shown for example by Enomoto et al.

Regarding claims 8 and 10-13, Gerber et al. do not specifically teach depositing the first conductor material in an amount that does not extend above the upper surface of the insulating substrate. It would have been well within the purview of one of ordinary skill in the art at the time the invention was made to deposit the first conductor material taught by Gerber et al. as modified by either one of Bohn or Johnston and Enomoto et al. in an amount that does not extend above the upper surface of the insulating substrate as opposed to an amount wherein part of the conductor extends above the upper surface of the insulating surface as both were well known equivalent alternatives in the art as shown for example by Enomoto et al. wherein depositing in an amount the does not extend above the upper surface of the insulating surface is advantageous in that no grinding is required.

Regarding claims 6, 7, and 14, Gerber et al. do not specifically teach forming the insulating substrate from glass-cloth epoxy, it being noted Gerber et al. is not limited to any material. It would have been obvious to one of ordinary skill in the art at the time the invention

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was made to form the insulating layer taught by Gerber et al. as modified by either one of Bohn or Johnston and Enomoto et al. from any well known and conventional insulating substrate material such as glass-cloth epoxy as shown for example by Enomoto et al. as only the expected results would be achieved.

Bohn and Johnston both disclose the well known methods for forming a multilayer printed circuit board by providing a stack of printed boards layers, i.e. insulating layers having conductors thereon, placing outermost conductor layers (e.g. copper foils) on the stack, interposing adhesive layers between all of the individual layers, laminating the stack to form a multilayer printed circuit board, and then etching the outermost conductor layers to form conductor circuits and thus, provide an integral, operable multilayer circuit board (Figure 1 and Column 1, lines 27-28, 50-54, and 65-66 and Column 3, lines 49-58 of Bohn and Figure 1 and Column 1, lines 11-19 and Column 4, lines 23-57 of Johnston). Bohn additionally teaches that in forming a multilayer circuit board the internal circuit board structures may be any that are desired it being only essential that the outer sides are covered by conductor layers (Column 1, lines 27-28 and Column 3, lines 56-58).

Enomoto et al. disclose a method for manufacturing a multilayer circuit board. Enomoto et al. teach forming a single circuit board by providing an insulating layer (e.g. formed of glass cloth epoxy resin) (e.g. 40 of Figures 3 and 7), forming a conductor layer (e.g. copper foil) on one side of the insulating layer (e.g. 42 of Figures 3 and 7), forming a via hole (e.g. 40a of Figures 3 and 7) (e.g. formed by laser processing) through the insulating layer to the conductor layer, covering the conductor layer with a protective film (48 of Figures 3 and 7), filling at least part of the via hole with a first electroplated conductor material (e.g. 46 of Figures 3 and 7)

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(wherein at least part of the upper surface of the conductor material is lower than the upper surface of the insulating substrate it being noted Enomoto et al. show both a first embodiment wherein at least part of the conductor material extends above the upper surface of the insulating substrate and a second embodiment wherein all of the first conductor material is below the upper surface of the insulating substrate the second embodiment having the advantage of not having to grind the first conductor material down to the upper surface of the insulating substrate), the conductor layer is used as one electrode during electroplating, and the protective film prevents altering the thickness of the conductor layer during plating, etching the conductor layer to form a conductor circuit (e.g. 32a of Figures 4 and 8), forming a conductive bump (e.g. 38a of Figure 4 and 460 of Figure 7) on the first conductor material from a second conductive material having a low melting point such that the bump projects from the upper surface of the insulating substrate, and placing a bonding layer (e.g. 34 of Figure 4 and 80 of Figure 8) over the conductive bump Enomoto et al. teach manufacturing a multilayer circuit board by applying heat and pressure to a multilayer stack of single circuit board layers (as described above) (Figures 3-5, 7, and 8 and Column 7, line 54-67 and Column 8, lines 8-9, 37-39, and 55-57 and Column 9, lines 15-65 and Column 10, lines 10-21 and 42-57 and Column 11, lines 32-35 and 58-67 and Column 12, lines 1-61).

#### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection. Applicants arguments regarding the new limitations are addressed above.

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***Conclusion***

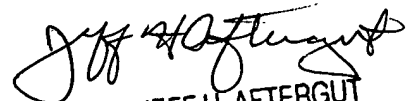
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on (571) 272-1171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John L. Goff



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